KROIX JONES

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EDUCATION

Howard University — B.S. Electrical Engineering, Minor in Mathematics: GPA: 3.77 Washington, DC | **May 2028**

Relevant Coursework: Digital Systems, Advanced Digital Systems, Circuit Theory, Engineering Programming, PCB Design,

SKILLS

Languages: Python, SystemVerilog, VHDL, Verilog, C/C++, Java, Kotlin, GO, MATLAB, Bash | **ML/Data:** PyTorch, scikit-learn, NumPy, pandas, SBERT, recommendation systems, cosine similarity, MMR, FastAPI, evaluation pipelines, GPU-aware optimization | **Hardware/Systems:** RTL design, RTL verification, testbenches, assertions, FPGA, Vivado, analog circuits, embedded systems, UART/serial, KiCad, Multisim, PSPICE, Git, Linux/UNIX, Cloud APIs.

EXPERIENCE

Hardware Systems Engineering Intern — Abbott Alameda, CA | May 2026–Aug 2026

- Support medical-device hardware and systems efforts for **PCBA- and ASIC-related Abbott Diabetes Care platforms**, including **analog circuit evaluation**, oscilloscope-based signal inspection, and hardware debug workflow development.
- Contribute **Go** code to **cloud API services connecting healthcare providers, patients, and Abbott administrators**, programming device/data workflow needs into backend service requirements.
- Built Python automation to analyze **~7.46M multichannel sensor readings** from 19 lab tests, replacing manual Plotly graph review with **structured event detection/reporting** and reducing inspection time by **~80%**.
- Implemented multi-channel phenomenon logic for **spikes, data loss, bias/align states, and long/short anomalies**, helping separate isolated sensor behavior from synchronized system-wide signal movement.
- Collaborate with embedded software, hardware, and data teams to connect lab hardware behavior with **data collection, debugging, and device-analysis needs**.

Implementation Automation Engineer — M6IT Consulting Remote / Manhattan, NY | Sep 2025–Apr 2026

- Built backend APIs, cloud API integrations, and automation tools for NDA-protected client software systems using **Java, Kotlin, SQL, and Python.**
- Developed Java/Python backend fixes, **debugging utilities, and data-processing scripts to improve reliability**, feature delivery, and operational turnaround.
- Supported ML/data automation work using Python, including **preprocessing, model prototyping, and algorithm optimization** for client-facing solutions totalling **$2+ million dollars in revenue** for the company.

Process Engineering Intern — Abbott Altavista, VA | May 2025–Aug 2025

- Built data-driven engineering presentation delivered to **North America VP of Nutrition** after collecting input from engineering, maintenance, lab, and plant leadership.
- Conducted field inspections and test work to prioritize **95% of plant inspection systems**, supporting reliability planning and maintenance decisions.

PROJECTS

KRX Music — Research-Driven Music Recommendation Engine | Python, ML, FastAPI, SBERT Mar 2022–Present

- Built **4-year** research-driven recommendation engine that maps music taste using perceptual audio analysis, **384-dimensional SBERT embeddings**, vector similarity, metadata-aware ranking, and diversity optimization.
- Designed a multimodal ranking pipeline comparing signal-level audio behavior and text context to rank up to **220 candidate tracks/query** across relevance, novelty, and taste alignment.
- Developed Taste Neighborhoods, a **live learned taste-graph** interface where **neural-network output groupings** update after likes/dislikes and expose **user-conditioned genre topology**,confidence, purity, stability, label evidence, and taxonomy.
- Reduced projected monthly infrastructure cost from **~$700 to ~$30** by redesigned the recommender from brute-force candidate mapping toward a **deep-learning taste-neighborhood pipeline**, trading higher uncached latency for scalable deployment.
- Ran **30-day private alpha** with 24 testers receiving 10 recommendations/day; **100% agreed** KRX was more relevant than their usual music provider, with **92% strongly agreeing.**

RV32I RISC-V CPU Core + SystemVerilog Verification Suite | SystemVerilog, RTL, FPGA May 2026–Present

- Building modular single-cycle **RV32I CPU** with PC, instruction/data memory, decoder, control unit, register file, immediate generator, ALU, branch/jump logic, and writeback.
- Writing module-level and CPU-level **SystemVerilog testbenches, directed instruction tests, assertions, waveform-debug notes**, and verification plan for FPGA deployment.
- Implementing **Python-assisted simulation workflows and regression checks** to validate instruction behavior, isolate RTL bugs, and improve repeatable CPU-level verification before FPGA deployment.

XIAO Scope Studio — Desktop Oscilloscope + Signal Generator | Python, Serial, Embedded Tools Apr–May 2026

- **Built and open-sourced a fully working oscilloscope/signal-generator app** for Seeed Studio XIAO SAMD21 hardware with serial handling, waveform capture, AWG generation, pin-map viewing, autosave, and packaged .exe distribution.
- Implemented live breadboard waveform capture, AWG signal generation, serial-device handling, runtime recovery, autosave history, pin map viewing, and a student-ready launcher workflow that **will be used in Howard's EE and CpE curriculum as of Fall 2026**

LEADERSHIP / HONORS

Howard University Achievers Scholar | Dean's List | IEEE Hands On PCB Engineering Chair | Sigma Phi Delta Programming Chair | Apple Next Generation Innovators | Ballet and Books Social Media Director | NSBE | PEPCO Scholar 2025-2026